WHAT IS CLAIMED IS

1. A semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, wherein:

a topmost stacked structure of the multilayer interconnect structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of high dielectric constant inorganic filler and insulating resin and including chip connection pads for directly connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip.

2. A semiconductor package, comprised of an insulating substrate on top and bottom surfaces of which multilayer interconnect structures are provided, for mounting a semiconductor chip on the top surface of a top surface multilayer interconnect structure, wherein:

the top surface multilayer structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of high dielectric constant inorganic filler and insulating resin, and a topmost layer of said top surface multilayer interconnect structure includes chip connection pads for connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip inside a region superposed with said capacitor structure in a plan view.

3. A semiconductor package as set forth in claim 2, wherein said top surface multilayer interconnect structure includes a plurality of stacked capacitor structures.

4. A semiconductor package as set forth in any one of claims 1 to 3, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

5. A semiconductor package as set forth in any one of claims 1 to 3, wherein said insulating resin is a polyimide resin.

6. A semiconductor device comprised of a semiconductor package as set forth in any one of claims 1 to 3 and a semiconductor chip directly connected at its electrodes to the chip connection pads.

7. A method of production of a semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, comprising:

a step of forming a capacitor structure in a topmost stacked structure of said multilayer interconnect structure,

said capacitor structure formation step comprising:

processing for forming at a bottommost layer of said topmost stacked structure a conductor layer for bottom electrodes of said capacitor structure,

processing for forming on said bottom electrodes by electrodeposition using an electrolyte comprised of high dielectric constant inorganic filler and insulating resin dispersed in a colloidal state a mixed electrodeposited layer of said inorganic filler and said insulating resin as a dielectric layer of said capacitor structure,

processing for forming on said dielectric layer a conductor layer for top electrodes of said capacitor structure, and

processing for forming inside said capacitor structure chip connection pads for directly connecting said top electrodes and said bottom electrodes with electrodes of said semiconductor chip.

8. A method of production of a semiconductor package, comprised of an insulating substrate on top and bottom surfaces of which multilayer interconnect structures are provided, for mounting a semiconductor chip on the top surface of a top surface multilayer interconnect structure, comprising:

a step of forming a capacitor structure in

a top surface multilayer interconnect structure,

said capacitor structure formation step comprising:

processing for forming a conductor layer for bottom electrodes of said capacitor structure,

processing for forming on said bottom electrodes by electrodeposition using an electrolyte comprised of high dielectric constant inorganic filler and insulating resin dispersed in a colloidal state a mixed electrodeposited layer of said inorganic filler and said insulating resin as a dielectric layer of said capacitor structure,

processing for forming on said dielectric layer a conductor layer for top electrodes of said capacitor structure, and

processing for forming chip connection pads for connecting said top electrode and said bottom electrode with electrodes of said semiconductor chip in a region of the topmost layer of said top surface multilayer interconnect structure superposed with said capacitor layer in a plan view.

9. A method of production of a semiconductor package as set forth in claim 8, further including a step of forming said capacitor structure by stacking a plurality of layers.